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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,976	10/31/2003	Prabir C. Maulik	A0312.70494US00	8831

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EXAMINER	
LEE, SIU M	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,976	MAULIK ET AL.	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/25/2005*., *8/27/2004*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the two current mirrors (current mirror 30 and current mirror 32) in figure 5 is unclear. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

Paragraph 0035, lines 2,and 12 recite FIGS 5a and 5b. With respect to the drawing, there are no figure 5a and 5b. The correct figure number should be 6a and 6b.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Cho (US 6,741,195 B1).

(1) Regarding claim 1:

Cho discloses a DAC (digital to analog converter in figure 1) receiving a digital input (a current having a magnitude corresponding to the value of a digital signal flows through a resistor to generate a voltage having a magnitude corresponding to the digital signal, column 1, lines 18-21) and providing an analog output (the curve 1 in figure 4 show the analog output from the DAC in figure 1, column 5, lines 30-53); wherein the line driver is reconfigurable between a current mode of operation (if the current is steered through the second switching transistor 124, the current contribute to the output current Iout* in figure 1, column 1, lines 56-58) and a voltage mode of operation (if the

current is steered through the first switching transistor 122, the current contributes to the current Iout flowing through the resistor R and generate a voltage output Vout, column 1, lines 54-56).

(2) Regarding claim 2:

Cho discloses wherein the current mode of operation includes first or second current sub-modes of operation (the current flowing through the mirror transistor 120 is steered through either a first switching transistor 122 or a second switching transistor 124 depending on the value of IN and IN*, column 1, lines 51-58).

(3) Regarding claim 3:

Cho discloses a DAC wherein the DAC provides a current output (the current output Iout* in figure 1, column 1, lines 56-58).

(4) Regarding claim 4:

Cho discloses wherein the current output is used to drive the line directly (the output of the DAC 502 and 504 and 506 are used to drive the line directly in figure 8, column 9, lines 36-38).

(5) Regarding claim 8:

Cho discloses that wherein the DAC includes full-scale current which is programmable (the DAC in figure 1 can be programmable to generate respective currents of I, 2I, 4I, and 8I depending of the input signal IN and IN*, column 1, lines 35-41).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,741,195 B1) in view of Gorecki (US 5,493,205).

(1) Regarding claim 5:

Cho discloses all the subject matter as discuss in claim 3 except further comprising a current mirror coupled between the DAC and the line that mirrors the current output of the DAC.

However, Gorecki discloses a current mirror (current mirror 60' in figure 5, column 6, lines 62-64).

It is desirable to further comprising a current mirror coupled between the DAC and the line that mirrors the current output of the DAC because it controls distortion of the current mirror by removing transistor threshold mismatches from effecting the distortion (column 3, lines 40-42). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the current mirror of Gorecki in the system of Cho to improve the performance of the system.

(2) Regarding claim 6:

Gorecki further disclose that the current mirror adds gain to the current output of the DAC (the switch 120 in the current mirror controls the gain of the current mirror, column 7, lines 9-30).

(3) Regarding claim 7:

Gorecki further discloses wherein the gain of the current mirror is programmable (the programmable output resistance of the current mirror 60' is determine by the switches 120 and by different stage of the switches 120 (on or off) the output resistance changes and thus can the gain of the current mirror, column 7, lines 1-30).

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,741,195 B1) in view of Mulder et al. (US 6,720,798 B2).

Cho discloses all the subject matter as discuss in claim 1 except wherein the driver includes a quiescent current which is programmable.

However, Mulder et al. discloses the driver (class AB digital to analog converter / line driver) includes a quiescent current which is programmable (column 7, lines 25-32).

It is desirable for the driver to includes a quiescent current which is programmable because it can reduce unwanted distortion (column 2, lines 20-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teaching of Mulder et al. with the system of Cho to improve the performance of the system.

8. Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,741,195 B1) in view of Zabroda (US 2004/006005 A1).

Cho discloses all the subject matter as discuss in claim 1 except wherein the line driver further including first and second current mirrors, first and second resistors, first

and second bipolar transistors, coupled between the DAC and the line, when the line driver operates in the voltage mode of operation.

However, Zabroda discloses a gigabit Ethernet line driver wherein the line driver further including first and second current mirrors, first and second resistors, first and second bipolar transistors, coupled between the DAC and the line, when the line driver operates in the voltage mode of operation (Zabroda discloses a gigabit Ethernet line driver that have both the transmitter output and the active hybrid output as shown in figure 1 in a voltage mode of operation, each transmitter cluster includes a plurality of transmitter cells consisting of a driver cell and digital to analog converter connected to driver cell. A hybrid circuit connects between the transmitter output and receiver input for separating a receiver from the transmitter signal responsive to a tuner signal. The transmitter consists of plurality of transmitter cluster and each cluster 100 ad 105 as shown in figure 3 contains three identical transmitter cells 125 as shown in figure 5 (paragraph 0032). Each transmitter cell 125 contains a DAC150 portion and a current mirror driver portion 155. Each current mirror portion 155 consists of two identical current mirror driver cells 180 as shown in figure 5 (paragraph 0033, lines 2-8). The detail of the hybrid portion 65 is shown in figure 8 wherein contains two resistors strings 225 and 230, the taps of the resistor string 225 and 230 are connected through a pair of transistor switches 235 in figure 8 (paragraph 0037, lines 1-9). Although the resistors shown in figure 8 is not bipolar transistor, it would be obvious to one of ordinary skill in the art to realize a FET transistor and a bipolar transistor can perform the same function).

It is desirable to have the driver further including first and second current mirrors, first and second resistors, first and second bipolar transistors, coupled between the DAC and the line, when the line driver operates in the voltage mode of operation because it provides power efficiency and lowered the non-linear distortion (paragraph 0008, lines 6-8 and paragraph 0009, lines 1-3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teaching of Zabroda with the DAC of Cho to improve the performance of the line driver.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cho (US 6,741,195 B1) in view of Rybicki (US 4,943,784).

Cho discloses all the subject matter as discuss in claim 1 except wherein the driver is configured to be placed on a high impedance state.

However, Rybicki discloses wherein the driver is configured to be placed on a high impedance state (Rybicki disclose a digital line driver 10 in figure 1 comprise a DAC 6 wherein the driver is configured to be placed on a high impedance state, column 3, lines 47-60).

It is desirable to configured the driver to be placed on a high impedance state because it improves the method of controlling operation of a line driver (column 1, lines 54-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teaching of Rybicki with the DAC of Cho to improve the controlling method of the line driver.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chaiken et al. (US 2002/0048109 A1) discloses a DB linear variable gain amplifier. Van Bavel et al. (US 6,665,347 B2) discloses a output driver for high speed Ethernet transceiver. Chan (US 2004/0005015 A1) discloses a method and system for a reduced emission direct drive transmitter for unshielded twisted pair (UTP) applications. Clara et al. (us 6,646,580 B2) discloses a digital/analog converter with programmable gain. Naviasky et al. (US 6,608,860 B1) discloses a low power dissipation, high linearity transmitter. Kearney et al. (US 5,608,348) discloses a binary programmable current mirror.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M. Lee
1/19/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER